

What is claimed is:

1. A system for synchronizing the operation of a transmitter clock and a local reference clock, said system comprising:

a transmitter block, said transmitter block for transmitting consecutive synchronization messages, each of said messages having a timestamp, said transmitter block maintaining a transmitter counter having a value, wherein each of said timestamps indicates said value of said counter at successive moments of time;

a receiver, coupled to said transmitter block, for receiving said synchronization messages; first and second synchronization registers, coupled to said receiver, said synchronization registers storing said timestamps of said consecutive synchronization messages;

a first comparator for comparing the values of said first and second synchronization registers to produce a synchronization time period;

first and second local reference registers, coupled to said local counter, each of said registers having a value indicative of a local reference counter at successive moments of time;

a second comparator, coupled to said first and second local reference registers, said comparator comparing the values of said first and second local registers and determining a local reference time period; and

a comparison and clock adjustment block, coupled to said first and second comparators and said local clock, said block comparing said synchronization time period with said local reference time period and then adjusting said local reference clock based upon said comparison.

2. The system of claim 1 wherein data is transmitted from said transmitter to said receiver, said system further comprising:

a processor block, coupled to said receiver, for determining the transmission rate of said data; and

5 a comparison and clock adjustment block, coupled to said local reference counter and said processor block, for adjusting said local reference counter based upon said determination of said rate.

3. The system of claim 2 wherein said comparison and clock adjustment block comprises a plurality of clock adjusters and CODEC clock generators, coupled to said processor block, for adjusting an digital-to-analog converter clock based upon said determination of said rate.

4. The system of claim 1 wherein said transmitter further comprises a controller, 15 said controller generating a strobe, said strobe delayed from the transmission of said data by a programmable amount.

5. The system of claim 1 wherein said transmitter also transmits a MAP message to said receiver, said MAP message instructing said receiver to create a message having a TDMA 20 format.

6. The system of claim 1 wherein said comparison and clock adjustment block includes a voltage controlled oscillator.

7. The system of claim 1 wherein said comparison and clock adjustment block includes a pulse stretcher.

8. A method for synchronizing two clocks of a first and second device comprising the steps of:

sending successive synchronization messages from said first device to said second device, said synchronization message having a timestamp;

receiving said successive synchronization messages at said second device and determining a synchronization period between said successive timestamps;

determining the period of said second clock of said second device;

comparing said synchronization period with said period of said second clock of said second device, wherein said comparison determines a difference; and

adjusting the period of said second clock based upon said difference.

9. The method of claim 8 comprising the further steps including:

sending data from the first device to the second device;

receiving said data at said second device;

determining the rate of the data; and

adjusting the rate of said second clock based upon said rate of said data.

10. The method of claim 9 wherein the rate of said second clock is adjusted using a voltage controlled oscillator.

11. The method of claim 9 wherein the rate of said second clock is adjusted using a pulse stretcher.

12. The method of claim 9 comprising the further steps of:
sending a MAP message from said first device to said second device, said MAP message instructing said second device to said first device in a TDMA format.

13. A cable modem, said cable modem adjusting the rate of a clock, said cable modem comprising:

a clock having a period;
means for receiving successive synchronization messages, each of said synchronization message containing a timestamp;
means for determining the period of said local clock;
a comparator for comparing the rate of said local clock with the period between successive timestamps in successive synchronization messages;
means for adjusting the period of said local clock based upon said comparison.

14. The cable modem of claim 13 further comprising:

means for receiving data;

means for determining the rate of said data; and

means for adjusting the rate of said local clock based upon said comparison.

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15. The cable modem of claim 13 wherein said comparator uses a voltage controlled oscillator.

16. The cable modem of claim 13 wherein said comparator uses a modulo comparator.

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17. A system comprising:

a hybrid fiber coax network;

a cable telephone modem (CTM) coupled to said hybrid fiber coax network, said modem

15 having a local clock;

a cable modem termination system (CMTS) coupled to said hybrid fiber coax network and a packet network, wherein said CMTS includes means for sending successive synchronization messages, each of said synchronization messages having a timestamp, to said cable telephone modem;

20 wherein said cable telephone modem includes means for receiving said synchronization message and determining a synchronization period, wherein said synchronization period is the time between successive timestamps; means for determining the period of said local clock;

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